4.b.i. Gray to Binary Converter

Aim: - To develop verilog code and test bench code for verification of Gray to Binary converter and to perform simulation and synthesis.

Tools required:-Xilinx ISE design software 14.7

Program:-

Verilog code:-

```
module     graytobinary1(input   [3:0]G,output   [3:0]B);
assign    B[3] = G[3];
assign    B[2] = G[3] ^ G[2] ;
assign    B[1] = G[3] ^ G[2] ^ G[1];
assign    B[0] = G[3] ^ G[2] ^ G[1] ^ G[0] ;
endmodule
```

Verilog Test Bench code:-

```
module     graytobinary2;
        // Inputs
        reg     [3:0] G;
        // Outputs
        wire    [3:0] B;
        // Instantiate the Unit Under Test (UUT)
        graytobinary1 uut (
                .G(G),
                .B(B)
```

```
);
initial  begin
        // Initialize Inputs
        G = 0;
        // Wait 100 ns for global reset to finish
        #100;
        // Add stimulus here
         G = 0; #100;
         G = 1; #100;
         G = 2; #100;
          G = 3; #100;
         G = 4; #100;
         G = 5; #100;
         G = 6; #100;
         G = 7; #100;
         G = 8; #100;
         G = 9; #100;
         G = 10; #100;
         G = 11; #100;
         G = 12; #100;
         G = 13; #100;
         G = 14; #100;
         G = 15; #100;
```

```
    end

endmodule
```

Block Diagram of Gray to Binary Converter:-

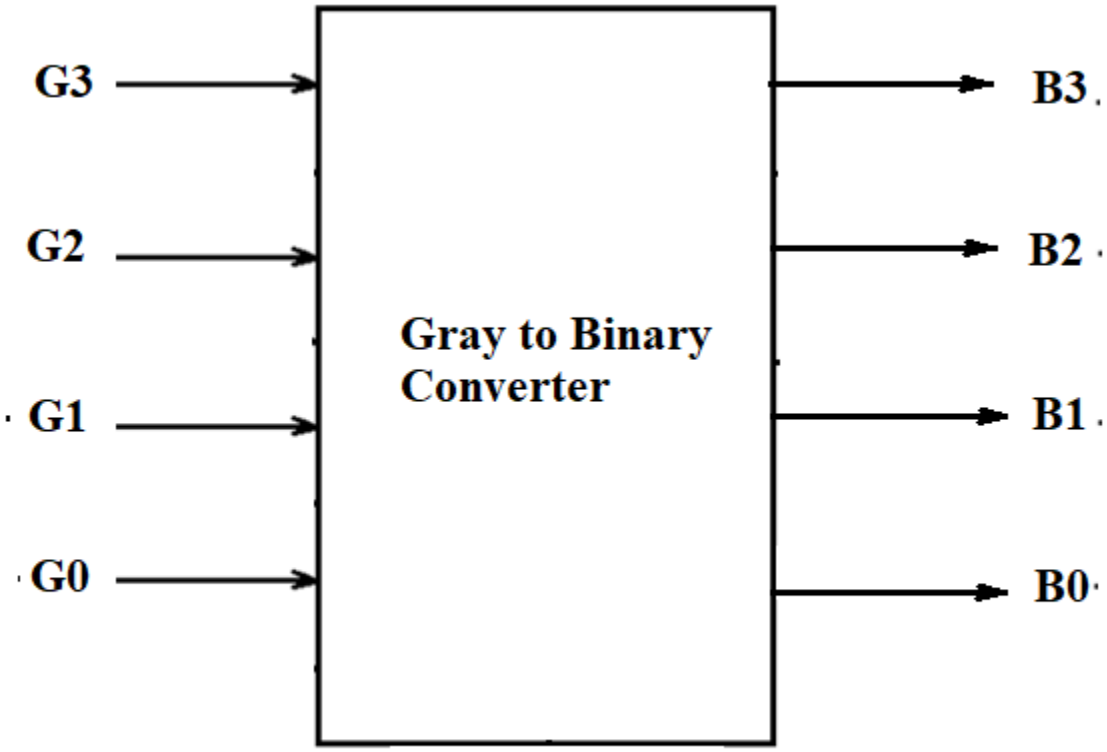

Fig: Gray to Binary Converter

Logic Diagram of Gray to Binary Converter:-

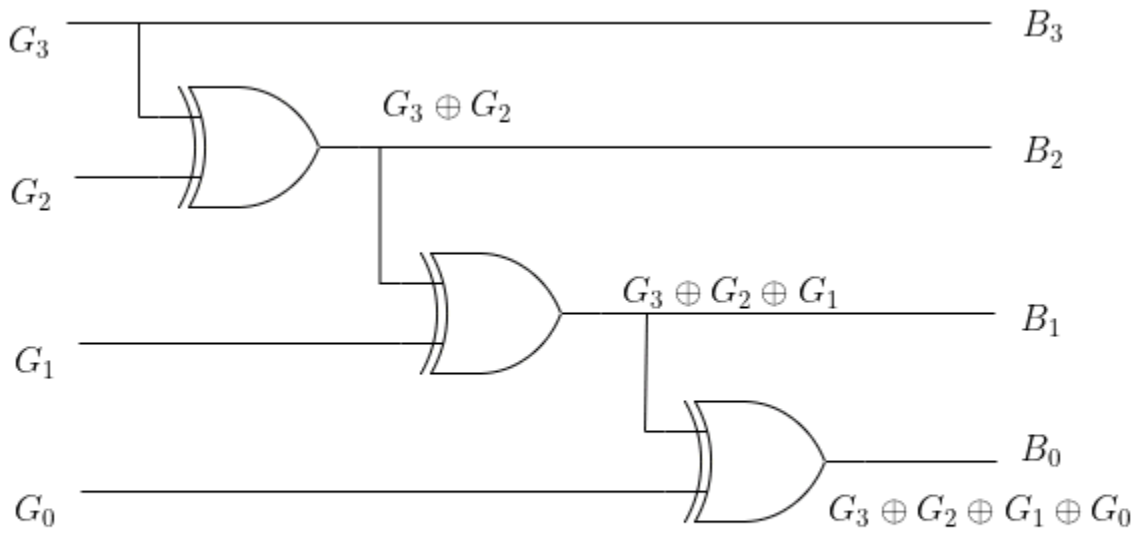

Fig: Gray to Binary Converter

Truth Table of Gray to Binary Converter:-

G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

Device utilization Summary:-

Timing Summary:-

Procedure:-

1. Switch on computer and double click on ISE project navigator icon.
2. In project Navigator window create a project by clicking file→ New project→ give project name→save the file.
3. Create a Verilog Module by right click on project name →select New Source→select verilog→give the name of the file.It creates .V file.
4. Write the Logic of the Module in the .V file and save it.
5. In design window right click on Verilog Module and select set as Top module for simulation.
6. In process window click on '+' symbol of synthesize –XST and double click on check syntax for syntax verification.
7. If No errors double click on view RTL Schematic and view Technology schematic one by one and capture Screenshot of schematics.
8. In design window, select simulation, right click on project name→select new source→select Verilog test fixture → give the name of the file. It creates verilog Test bench code.
9. In add stimulus here in Test bench code Enter corresponding input combinations.
10. Click on simulation (or in design window select verilog test bench, then click on '+' symbol of Isim simulator), double click on behavioral check syntax for verification.
11. Double click on simulate behavioral model for output waveform.
12. In implementation process double click on design summary process window.
13. Click on synthesis report in right side window and note down device utilization summary and timing diagram Summary.

Result:- The Verilog code and Test bench code for Gray to Binary Converter was developed and verification of synthesis and simulation was performed.