8.a. Parallel In Parallel Out

Aim: - To develop VHDL code and Test bench code for verification of Parallel In Parallel Out (PIPO) shift register and to perform simulation and synthesis.

Tools required:-Xilinx ISE design software 14.7

Program:-

VHDL code:-

```
library ieee;
use ieee.std_logic_1164.ALL;
entity pipo is Port ( u : in std_logic_vector (5 downto 0);
clk : in std_logic;
rst : in std_logic;
w : out std_logic_vector (5 downto 0));
end pipo;
architecture Behavioral of pipo is
begin
process(u,clk,rst)
begin
if(rst='1')then
w <= "000000";
elsif(clk'event and clk='1')then
w(0) <= u(0);
w(1) <= u(1);
```

```
w(2) <= u(2);
w(3) <= u(3);
w(4) <= u(4);
w(5) <= u(5);
end  if;
end  process;
end   Behavioral;
```

Block Diagram of PIPO:-

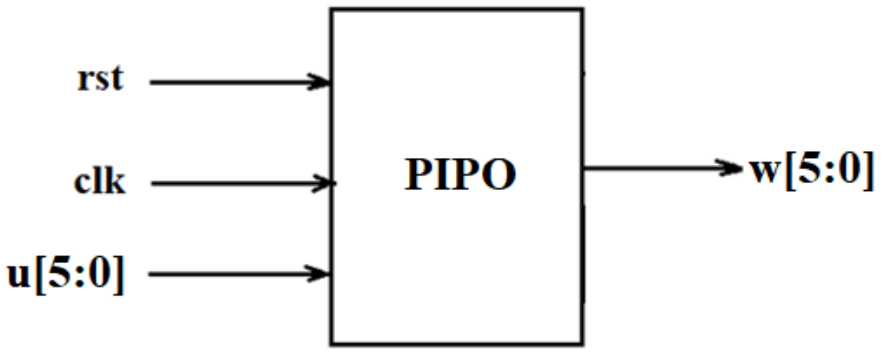


Fig: Parallel In Parallel Out Shift Register

Truth Table of PIPO:-

clk	rst	u[5:0]	W[5:0]
1	0	101101	101101
1	0	111111	111111
1	0	100100	100100
1	1	101110	000000

Device utilization Summary:-

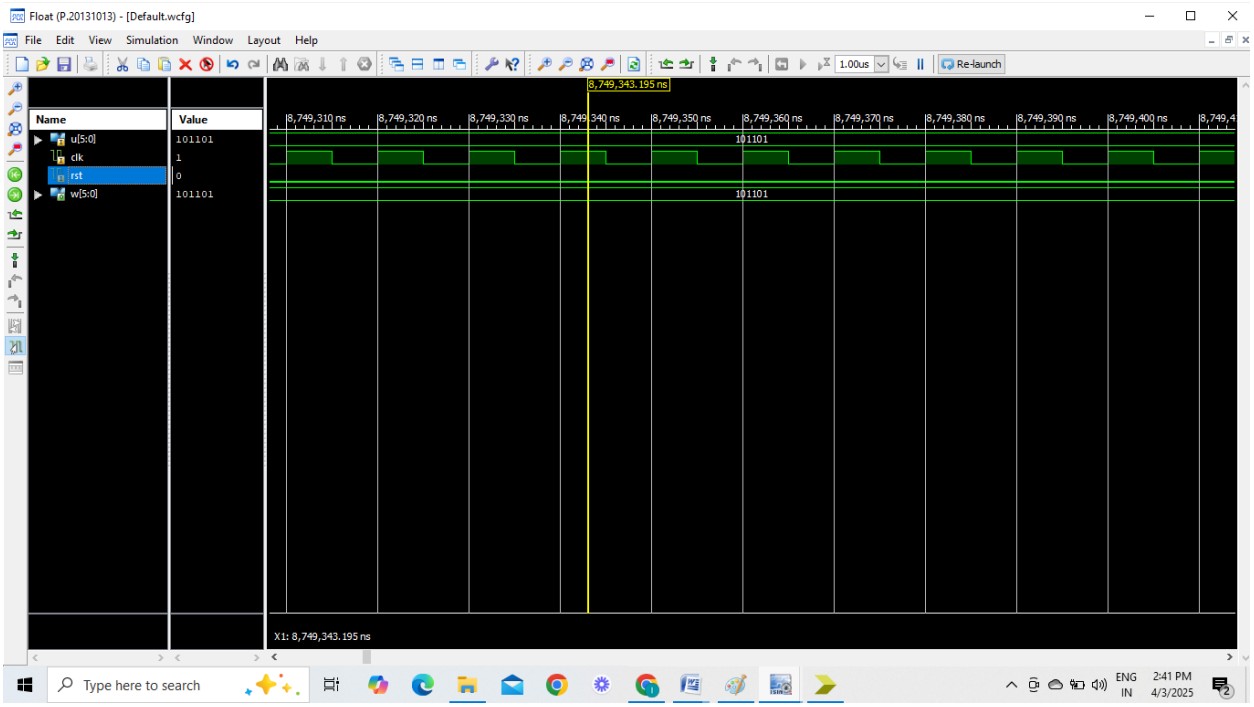
Timing Summary:-

Procedure:-

1. Create a New project.
2. Create a VHDL Module (pipo) ,Write the Logic of the module and save it.
3. In design window right click on VHDL Module and select set as Top module for simulation.
4. Under Implementation select VHDL modules perform synthesize – XST and check syntax for syntax verification.
5. Observe RTL Schematic and Technology schematics.
6. Under Simulation select main module (pipo), perform behavioral check syntax for verification and simulate behavioral model for output waveform.
7. Observe output waveforms by using Force values to rst, clk,u.
8. In Design process Observe Device utilization, Timing summaries.

Result:- The VHDL code and Test bench code for PIPO was developed and verification of synthesis and simulation was performed.

Output waveforms:- PIPO



8.b.Serial In Parallel Out

Aim: - To develop VHDL code and Test bench code for verification of Serial In Parallel Out (SIPO) shift register and to perform simulation and synthesis.

Tools required:-Xilinx ISE design software 14.7

Program:-

VHDL code:-

```
library   ieee;

use   ieee.std_logic_1164.all;

entity sipo is

port(

clk, clear : in std_logic;

Input_Data: in  std_logic;

Q: inout   std_logic_vector(3 downto 0) );

end   sipo;

architecture   arch   of   sipo   is

begin

process (clk)

begin

if clear = '1' then

Q <= "0000";

elsif (clk'event and clk='1') then

Q(3 downto 1) <= Q(2 downto 0);
```

```
Q(0) <= Input_Data;
end  if;
end   process;
end  arch;
```

Block Diagram of SIPO:-

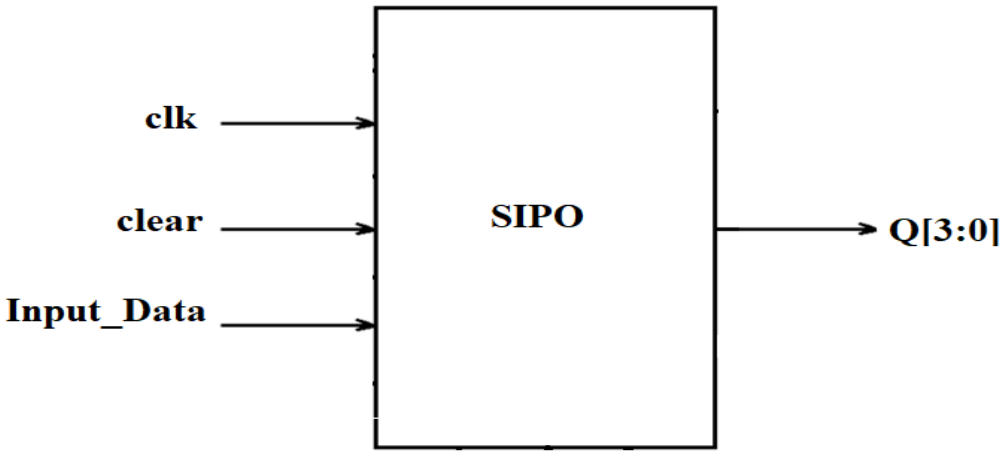


Fig: Serial In Parallel Out Shift Register

Truth Table of SIPO:-

clk	clear	Input_Data	Q[3:0]
1	0	1	1111
1	0	0	0000
1	1	0	0000
1	1	1	0000

Device utilization Summary:-

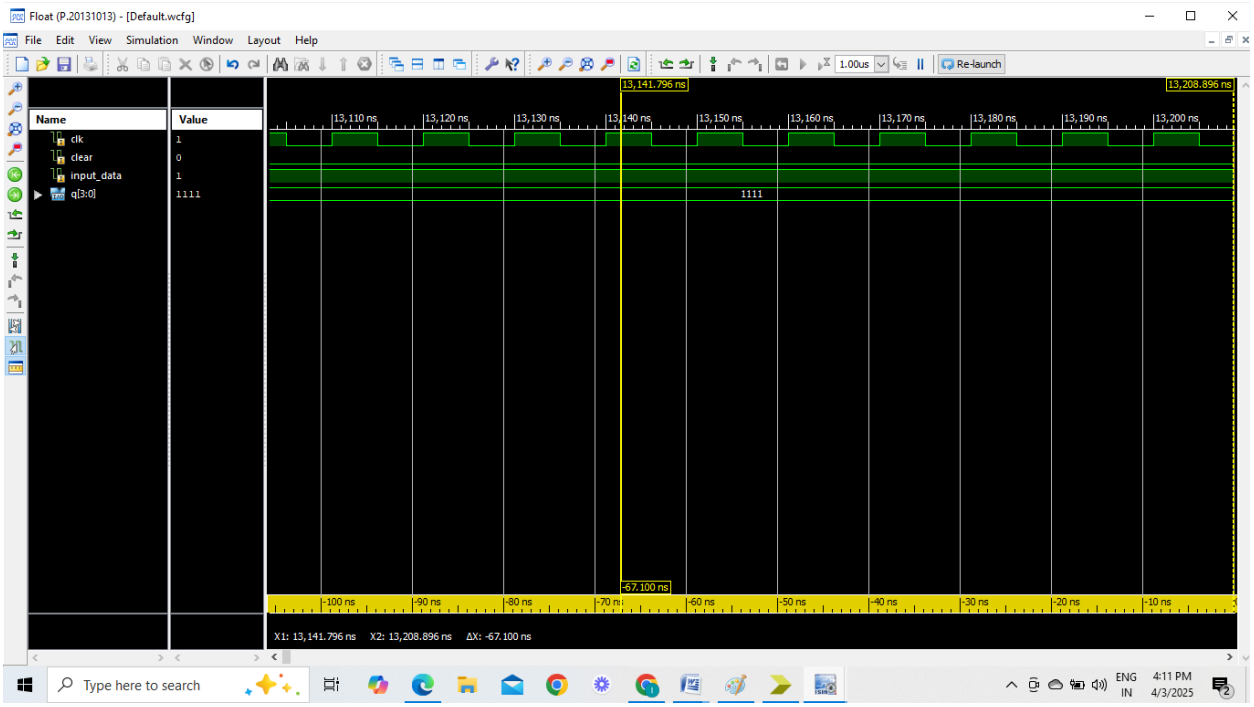
Timing Summary:-

Procedure:-

1. Create a New project.
2. Create a VHDL Module (sipo) ,Write the Logic of the module and save it.
3. In design window right click on VHDL Module and select set as Top module for simulation.
4. Under Implementation select VHDL modules perform synthesize – XST and check syntax for syntax verification.
5. Observe RTL Schematic and Technology schematics.
6. Under Simulation select main module (sipo), perform behavioral check syntax for verification and simulate behavioral model for output waveform.
7. Observe output waveforms by using Force values to clk,clear,Input_Data.
8. In Design process Observe Device utilization, Timing summaries.

Result:- The VHDL code and Test bench code for SIPO was developed and verification of synthesis and simulation was performed.

Output waveforms:- SIPO



8.c.Serial In Serial Out

Aim: - To develop VHDL code and Test bench code for verification of Serial In Serial Out (SISO) shift register and to perform simulation and synthesis.

Tools required:-Xilinx ISE design software 14.7

Program:-

VHDL code:-

```
library     ieee;
use    ieee.std_logic_1164.all;
entity   siso  is
port (clk : in   std_logic;
rst : in    std_logic;
sin : in    std_logic;
sout : out  std_logic);
end   siso;
architecture  s1  of  siso  is
begin
process(clk,rst,sin)
begin
if(rst='1') then
sout <= '0';
elsif(clk='1' and clk'event) then
sout <= sin;
```

```
end   if;

end   process;

end  s1;
```

Block Diagram of SISO:-

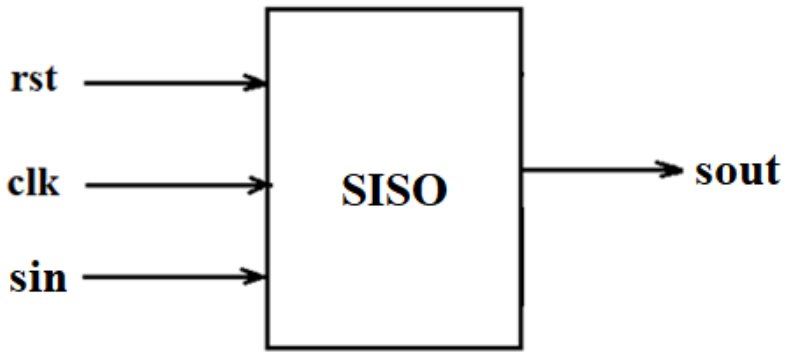


Fig: Serial In Serial Out Shfit Register

Truth Table of SISO:-

clk	rst	sin	sout
1	0	0	0
1	0	1	1
1	1	1	0

Device utilization Summary:-

Timing Summary:-

Procedure:-

1. Create a New project.
2. Create a VHDL Module (siso) ,Write the Logic of the module and save it.
3. In design window right click on VHDL Module and select set as Top module for simulation.
4. Under Implementation select VHDL modules perform synthesize – XST and check syntax for syntax verification.
5. Observe RTL Schematic and Technology schematics.
6. Under Simulation select main module (siso), perform behavioral check syntax for verification and simulate behavioral model for output waveform.
7. Observe output waveforms by using Force values to rst, clk,sin.
8. In Design process Observe Device utilization, Timing summaries.

Result:- The VHDL code and Test bench code for SISO was developed and verification of synthesis and simulation was performed.

Output waveforms:- SISO