

4.a. 8 to 1 Multiplexer

Aim: - To develop verilog code and test bench code for verification of 8 to 1 Multiplexer and to perform simulation and synthesis.

Tools required:-Xilinx ISE design software 14.7

Program:-

Verilog code:-

```
module Multiplexer8X1_1(S,I,Y);  
input [2:0]S;  
input [7:0]I;  
output Y;  
reg Y;  
always@(S,I)  
begin  
case(S)  
3'b000:Y = I[0];  
3'b001:Y = I[1];  
3'b010:Y = I[2];  
3'b011:Y = I[3];  
3'b100:Y = I[4];  
3'b101:Y = I[5];  
3'b110:Y = I[6];  
3'b111:Y = I[7];
```

```
endcase
```

```
end
```

```
endmodule
```

Verilog Test Bench code:-

```
module Multiplexer8X1_2;
```

```
    // Inputs
```

```
    reg [2:0] S;
```

```
    reg [7:0] I;
```

```
    // Outputs
```

```
    wire Y;
```

```
    // Instantiate the Unit Under Test (UUT)
```

```
    Multiplexer8X1_1 uut (
```

```
        .S(S),
```

```
        .I(I),
```

```
        .Y(Y)
```

```
    );
```

```
    initial begin
```

```
        // Initialize Inputs
```

```
        S = 0;
```

```
        I = 0;
```

```
        // Wait 100 ns for global reset to finish
```

```
        #100;
```

```
// Add stimulus here
```

```
#100; S = 0;I = 2;
```

```
#100; S = 1;I = 4;
```

```
#100; S = 2;I = 6;
```

```
#100; S = 3;I = 8;
```

```
#100; S = 4;I = 10;
```

```
#100; S = 5;I = 12;
```

```
#100; S = 6;I = 14;
```

```
#100; S = 7;I = 16;
```

```
end
```

```
endmodule
```

Block Diagram of 8 to 1 Multiplexer:-

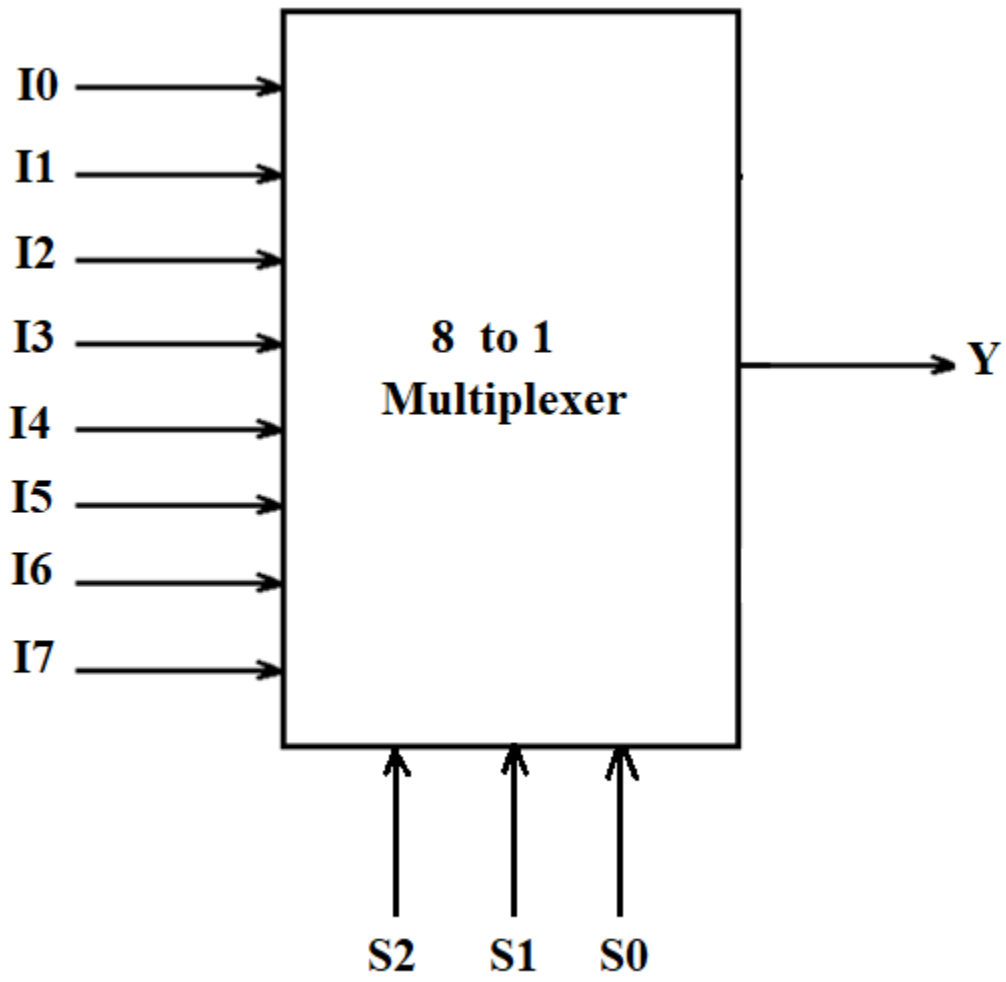


Fig: 8 to 1 Multiplexer

Logic Diagram of 8 to 1 Multiplexer:-

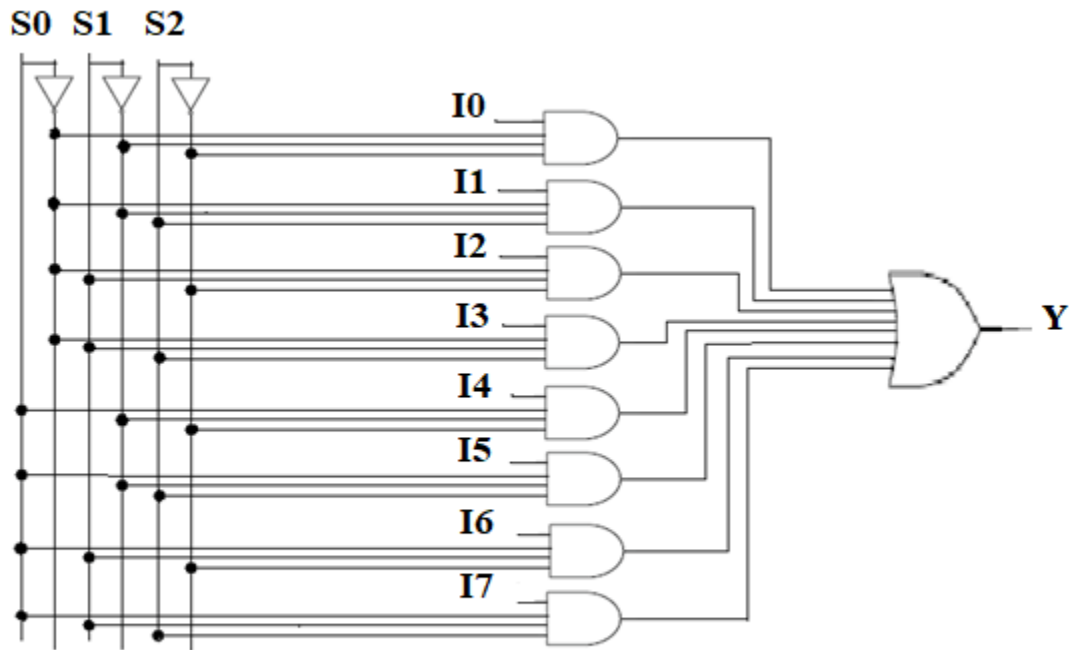


Fig: Logic diagram of 8 to 1 Multiplexer

Truth Table of 8 to 1 Multiplexer:-

S2	S1	S0	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

Device utilization Summary:-

Timing Summary:-

Procedure:-

1. Switch on computer and double click on ISE project navigator icon.
2. In project Navigator window create a project by clicking file→ New project→ give project name→save the file.
3. Create a Verilog Module by right click on project name →select New Source→select verilog→give the name of the file. It creates .V file.
4. Write the Logic of the Module in the .V file and save it.
5. In design window right click on Verilog Module and select set as Top module for simulation.
6. In process window click on '+' symbol of synthesize –XST and double click on check syntax for syntax verification.
7. If No errors double click on view RTL Schematic and view Technology schematic one by one and capture Screenshot of schematics.
8. In design window, select simulation, right click on project name→select new source→select Verilog test fixture → give the name of the file.It creates verilog Test bench code.
9. In add stimulus here in Test bench code Enter corresponding input combinations.
- 10.Click on simulation (or in design window select verilog test bench, then click on '+' symbol of Isim simulator), double click on behavioral check syntax for verification.
- 11.Double click on simulate behavioral model for output waveform.
- 12.In implementation process double click on design summary process window.
- 13.Click on synthesis report in right side window and note down device utilization summary and timing diagram Summary.

Result:- The Verilog code and Test bench code for 8 to 1 Multiplexer was developed and verification of synthesis and simulation was performed.